First Named Inventor: Joël Chatal Application No.: 10/616,226

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REMARKS

This Amendment is submitted in response to the Office Action mailed on December 6, 2004. Pending in the present application were claims 1, 2, 5, and 7-26. In the Office Action, objection was made to the specification and claims 5, 8, and 10 due to grammatical errors; claims 12-15 and 20-23 were rejected for failing to comply with the enablement requirement; and claims 1, 2, 5, 7-11, 16-19, and 24-26 were allowed. With this Amendment, the specification and claims 5, 8, and 10 are amended to correct the grammatical errors and overcome the objections thereto. In reliance on the following remarks, the present application containing claims 1, 2, 5, and 7-26 is now in condition for allowance, and notice to that effect is respectfully requested.

In the Office Action, dependent claims 12-15 and 20-23 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. "Any analysis of whether a particular claim is supported by the disclosure in an application requires a determination of whether that disclosure, when filed, contained sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention." M.P.E.P. § 2164.01. The enablement requirement has been interpreted to require that the claimed invention be enabled so that any person skilled in the art can make and use the invention without undue experimentation. M.P.E.P. § 2164.01 (citations omitted). Here, the present application, as originally filed, does provide a written description sufficient to enable one of skill in the art to practice the claimed invention without undue experimentation.

Dependent claims 12-15 and 20-23 are directed to a bandgap electrical reference voltage source having first and second current sources that produce respective first and second currents. The first and second currents are summed to create a reference current. According to the embodiment of these claims, a variation of the second current as a function of temperature does not compensate for a variation of the first current as a function of the temperature, such that the reference current does depend on the temperature.

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As noted in the Office Action, the reference current of claims 12-15 and 20-23 is the current through resistance R4 of FIG. 5. According to the specification, in one embodiment, a variation of current I6 (first current) as a function of temperature does not compensate for a variation of current I7 (second current) as a function of the temperature, such that the current through resistance R4 (reference current) varies as a function of the temperature. (Paragraphs 271-279; page 32, line 2 - page 33, line 11). The specification teaches that current I6 is produced by adding transistor M33 to current mirror 200 of FIGS. 2 and 4, with transistor M33 having its source and gate connected in parallel with the source and gate of transistor M3; i.e., having its source and gate respectively connected to the source and gate of transistor M3. (Paragraph 271; page 32, lines 2-7). Similarly, current I7 is produced by adding transistor M44 to current mirror 201 of FIGS. 2 and 4, with transistor M44 having its source and gate connected in parallel with the source and gate of transistor M44 having its source and gate connected in parallel with the source and gate of transistor M4. (Paragraph 276; page 32, lines 18-22).

The specification further teaches that the surface area of the gate of transistor M33 differs from the surface area of the gate of transistor M3, so that "the currents I4 and I6 output by transistors M3 and M33 respectively are different." (Paragraph 272; page 32, lines 8-13). The gates of transistors M4 and M44 have identical widths and lengths so that currents I5 and I7 are equal. (Paragraph 277; page 32, lines 23-26). As is known in the art, the current passing through a MOSFET transistor is proportional to the width of the gate of the device. (Paragraph 142; page 18, lines 18-28).

FIGS. 2 and 4 illustrate that transistors M3 and M4 output respective currents I4 and I5 via their drains connected to terminal 140 of resistance R3. (Paragraphs 139, 179, and 239; page 18, lines 7-9, page 23, lines 3-5, and page 29, lines 8-10). One skilled in the art would understand, without undue experimentation, that transistor M33 similarly outputs current I6 via its drain connected to terminal 540 of resistance R4 and M44 outputs current I7 via its drain connected to terminal 540 of resistance R4.

In sum, the present application teaches a structure to produce current I6 dependent upon temperature; namely, transistor M33 having its source and gate connected in parallel with the source and gate of transistor M3 of current mirror 200, and having a gate surface area different than that of transistor

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M3. The present application also teaches a structure to produce current I7 independent of temperature; specifically, transistor M44 having its source and gate connected in parallel with the source and gate of transistor M4 of current mirror 201, and having the width and length of its gate identical to the width and length of the gate of transistor M4. Accordingly, one of skill in the art could, without undue

experimentation, build the circuit of FIG. 5 with correct currents I6 and I7.

Because the written description provides disclosure is sufficient to enable one of skill in the art to practice the invention of claims 12-15 and 20-23, the rejection should be withdrawn. The application containing pending claims 1, 2, 5, and 7-26 is in condition for allowance. Reconsideration and notice to that effect is respectfully requested. The Examiner is invited to contact the undersigned at the telephone number listed below if such a call would in any way facilitate allowance of the application.

Respectfully submitted,

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Date: 2/1/05

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